Lab #17 Name: _____ Per: _____

Title: PARALLEL LOAD SHIFT REGISTER

Materials:
[2] 7476 dual J-K flip-flop ICs
[1] clock (single pulse)

Procedure:

1. Insert two 7476 ICs into the breadboard.
2. Wire the 4-bit, parallel load, recirculating, shift-register that was drawn in class. Use one input switch for the CLR and four input switches for the data (parallel load) inputs. Connect the single-pulse clock to the CLK inputs.
3. Clear data from the shift register by placing the CLR switch to 0 and then back to 1. This is shown in line 1 of Table 17-2.
4. Operate the shift register as shown in Table 17-2 and record the results. **Get Instructor's Signature (and be ready to explain how to load the shift register with a starting sequence).**

Questions: (answer on a separate piece of paper – **"Draw" means you must use a template**):

1. **Draw** a logic symbol diagram for a 5-bit, parallel load, recirculating, shift-right, register. Use five J-K flip-flops. Label the inputs CLR, CLK, and parallel data (A, B, C, D, and E). Label the outputs A, B, C, D, and E.
2. The parallel loading on the register you wired in this experiment was _____ (asynchronous, synchronous) loading.
3. Using the 7476 J-K flip-flop, the data was shifted on the _____ (negative, positive) –going edge of the clock pulse.
4. Parallel loading is sometimes called _____ (broadside, broadband, serial) loading.
5. If just output D were used, this circuit would be considered a parallel-in _____ (parallel, serial) –out register.

Inputs							Outputs			
Line	Clear	Parallel data				clock pulse number	LED indicators			
		A	B	C	D		A	B	C	D
1	0	1	1	1	1	0	0	0	0	0
2	1	0	1	1	1	0				
3	1	1	1	1	1	1				
4	1	1	1	1	1	2				
5	1	1	1	1	1	3				
6	1	1	1	1	1	4				
7	1	1	1	1	1	5				
8	0	1	1	1	1					
9	1	1	0	0	1					
10	1	1	1	1	1	6				
11	1	1	1	1	1	7				
12	1	1	1	1	1	8				
13	1	1	1	1	1	9				
14	0	1	1	1	1					
15	1	1	0	0	0					
16	1	1	1	1	1	10				
17	1	1	1	1	1	11				
18	1	1	1	1	1	12				
19	1	1	1	1	1	13				
20	0	1	1	1	1					
21	1	0	1	0	1					
22	1	1	1	1	1	14				
23	1	1	1	1	1	15				
24	1	1	1	1	1	16				
25	1	1	1	1	1	17				

Table 17-2 Parallel Shift Register